Circuit Simulation

Overall not a complex circuit, however a large amount of inputs. Suffer from licensing issues, whereas the software required to perform a professional level of analysis is unavailable. Had to make due with open source software and available software by breaking up and reformatting the problem.

**Power Testing**

Use LTSPICE – a robust open source version recommended in the course text and freely available from [4].

8 inputs of 6 bits each – Possible combinations are 248 = 281 trillion!

Impractical to test all possible combinations of inputs and outputs in spice. We still want to get an idea of the power consumption and delay the circuit.

Can use the bounding approach. Test all possible combinations of input vectors for each individual component and observe the power usage for the specific component. Can obtain:

* Min/avg/max power usage associated with the switching of each component.

Can multiply these min/avg/max values for each component by the number of components in the circuit. We can then obtain the worst-case power consumption for the overall circuit.

What is the effect of interconnect on power consumption?

Section 6.5

**Components:**

* Ripple-carry adder – 2 six-bit input vectors: 4096 possible combinations.
* Kogge-Stone adder – 2 six-bit input vectors: 4096 possible combinations.
* Ripple-Carry comparator – 2 six-bit input vectors: 4096 possible combinations.
* Kogge-Stone comparator – 2 six-bit input vectors: 4096 possible combinations.
* 2-input MUX 2 six-bit input vectors, 1 select line: Since it’s one or the other, can simplify to 1 six-bit input vector and one select line: 128 possible combinations.

**Input Waveform:**

Pulse sources are convenient for repetitive signals like clocks. The general form for a pulse source is illustrated in Figure 8.3. For example, a clock with a 1.0 V swing, 800 ps period, 100 ps rise and fall times, and 50% duty cycle (i.e., equal high and low times) would be expressed as [1]

<name> (+terminal –terminal) vsource type=pulse

val0=v1 val1=v2 delay=td rise=tr fall=tf width=pw period=per

* Need to hold values high long enough to obtain a stable output.

- Input vector generation oscillating vectors [1].

**Analysis:**

- Can compare min/avg/max power consumption of all the adders. Each one has a different graph with all four components together.

* Can SPICE output CVS data so it can be put into a graph in Excel? Or does it have to be done in the program itself? - YES [2]

- Compare min/avg/max of the speed vs power adder.

- dB gain compared to uncoded signal.

**Propagation Delay Testing**

Two types of delay timing analysis: Static and dynamic timing.

**Dynamic Testing:**

**Static testing:**

* The main advantage of STA over vector-based timing simulation is that it does not rely on input vectors [8].
* The basic STA algorithm is linear in runtime with circuit size [8].
* The basic STA analysis is conservative in the sense that it will overestimate the delay of long paths in the circuit and underestimate the delay of short paths in the circuit [8].
* This makes the analysis “safe,” guaranteeing that the design will function at least as fast as predicted and will not suffer from hold-time violations [8].

Due to the low algorithmic complexity and conservative nature of STA analysis, it was determined that a static timing analysis would be the best.

Typical STA analysis can be done using ETS from Cadence and Primetime from Synopsis [3]. Due to licensing issues these were unfortunately unavailable, so we had to employ a potpourri of different softwares.

**Gate Delay**

Delay characterization for cell libraries is clearly defined [8].

Use the FO4 test set up in chapter 8 of the text.

* Do FO4 analysis for each gate to obtain timing analysis

**Interconnect Delay:**

Can extract the length and width of the wires from the layout.

**Component Delay**

* Static timing can be done via a node-weighted directed graph [7]
* where the node weights represent the delay for each individual component and the path weights represent the π-model representation of the interconnect
* Once STA completed for each main component, can perform on

**Circuit Delay**

The solution of the differential equation is called the *transient response*, and the delay is the time when the output reaches *VDD* /2. [3]

Need to load the circuit to avoid bootstrapping.

Net delays are calculated based on the Wire Load Models(WLM) or extracted resistance R and capacitance C. Wire Load Models(WLM) are available in the Technology File. These values are Table Look Up(TLU) values calculated based on the net fanout length [6].

One of the simplest measures of a process’s inherent speed is the fanout-of-4 inverter delay. [1]

* Section 8.2.4 in the text covers how to model FO4 simulation delay. As well as example propagation delay netlist.
* Section 8.5.3 in the course text covers logical effort of simulations.

Research exact definition of FO4 delay

Static timing analyzer: 4.6 and 14.4.1.4

Verify how to do FO4 delay in LTSPICE

WIRE DELAY IS IMPORTANT - Does ELECTRIC Layout generate capacitance/resistance for wires?

* Section 8.6.
* 4 segment π-model is sufficient to represent interconnects [3]

Identify the critical path by hand.

Find longest path from book – Then measure what the propagation delay is to obtain the delay for the specific circuit.

* In practice, circuit designers depend on both hand analysis and simulation, or as [Glasser85] puts it, “simulation guided through insight gained from analysis.” [3]

Assume all inputs have been pushed in and are held constant in latches. Trellis circuit is purely combinational so we just want to see how long the propagation delay is.

Pin to pin delay of individual components?

Find longest delay of all components.

Create a graph and do an edge weight analysis to find the shortest and longest path?

**References**

[1] [www.cems.uvm.edu/~txia/Tutorial\_guide\_**stimulus**.pdf](http://www.cems.uvm.edu/~txia/Tutorial_guide_stimulus.pdf)

[2] <http://www.linear.com/solutions/1815>

[3] course text

[4] <http://www.linear.com/designtools/software/>

[5] <http://www.vlsi-expert.com/2011/03/static-timing-analysis-sta-basic-timing.html>

[6] <http://asic-soc.blogspot.ca/2008/08/dynamic-vs-static-timing-analysis.html>

[7] <https://embedded.eecs.berkeley.edu/eecsx44/lectures/Spring2013/timingAnalysis.pdf>

[8] Statistical Timing Analysis: From Basic Principles to State of the Art.